EPFL Workshop on Logic Synthesis and Verification

Thursday, 10 December 2015

Session: Advances in Logic Synthesis

9:00-9:20 **Why Again Logic Synthesis?**
Giovanni De Micheli (EPFL)

9:20-9:40 **Automatic Pipelining During Sequential Logic Synthesis**
Jordi Cortadella (*Universita Politècnica de Catalunya*)

9:40-10:00 **Component-based Synthesis by Solving Language Equations**
Tiziano Villa (*University of Verona*)

10:00-10:30 **Discussion**

10:30-11:00 *Coffee break*

11:00-11:20 **The Majority Logic Optimization Paradigm**
Luca Amaru (*EPFL*)

11:20-11:40 **Fast Synthesis: DC Explorer Perspective**
Jovanka Ciric-Vujkovic (*Synopsys*)

11:40-12:00 **Logic Synthesis via Boolean Relations**
Valentina Ciriani (*University of Milano*)

12:00-12:30 **Discussion**

12:30-14:00 *Lunch*

Session: Logic Synthesis and Verification

14:00-14:20 **Synthesis for Verification**
Robert Brayton *(UC Berkeley)*

14:20-14:40 **Verification of Arithmetic Circuits: What Makes it Difficult?**
Maciej Ciesielski (*University of Massachusetts, Amherst*)

14:40-15:00 **Using Formal Techniques for Design for Verifiability**
Rolf Drechsler (*University of Bremen*)

15:00-15:30 **Discussion**

15:30-16:00 *Coffee break*

16:00-16:20 **Logic Synthesis, Verfification and Test for Secure ICs**
Igor Markov (*University of Michigan*)

16:20-16:40 **Syntax-Guided Synthesis for Accurate RTL Error Localization and Correction**
Paolo Ienne (*EPFL*)

16:40-17:00 **Synthesis Inside Satisfiability Modulo Theory Solvers**
Viktor Kuncak (*EPFL*)

17:00-17:30 **Discussion**

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Session: Logic Synthesis for Alternative Technologies

9:00-9:20 **Index Generation Functions: Logic Synthesis for Pattern Matching**
Tsutomu Sasao (*Meiji University, Kanagawa*)

9:20-9:40 **Logic Synthesis in the Twilight of Moore's Law - Near-threshold, Heterogeneous, 3D Design Looking for a New Toolbox**
Luca Benini (*ETHZ*)

9:40-10:00 **Optimization of Robust Asychronous Threshold Networks Using Local Relaxation Techniques**
Steven Nowick (*Columbia University*)

10:00-10:30 **Discussion**

10:30-11:00 *Coffee break*

11:00-11:20 **Formal Approaches to Safe Software Development for Medical Devices**
Alena Simalatsar (*EPFL*)

11:20-11:40 **Viable Paths Towards Graphene Circuits: Implementation Styles and Logic Synthesis Tools**
Enrico Macii (*Politecnico di Torino*)

11:40-12:00 **EDA 3.0: Time to Refactor Logic Synthesis**
Leon Stok (*IBM*)

12:00-12:30 **Discussion**

12:30-14:00 *Lunch*

Session: Hardware Acceleration for Synthesis & Synthesis for Hardware Acceleration

14:00-14:20 **Synthesis for Hardware Acceleration**
Jason Cong (*UCLA*)

14:20-14:40 **Automatic Time Sharing for Area Reduction in FPGA Synthesis**
Henri Fraisse (*Xilinx*)

14:40-15:00 **Will FPGA Reconfiguration Change the Synthesis Problem?**
Dirk Stroobandt (*Ghent University*)

15:00-15:30 **Discussion**

Closing Keynote

15:30-16:00 **The Evolution of Synthesis - Dots and Dashes…Zeros and Ones**
Antun Domic (*Synopsys*)